The Use of Silicon-Germanium Superlattices for Thermoelectric Devices and Microfabricated Generators

L. Ferre Llin[a], F. Mirando[a], A. Samarelli[a], A. Odia[a], S. Cecchi[b], T. Etzelstorfer[c], E. Müller Gubler[d], D. Chrastina[b], G. Isella[b], J. Stangl[c], J.M.R. Weaver[a], P.S. Dobson[a] and D.J. Paul[a]

[a] University of Glasgow, School of Engineering, Rankine Building, Oakfield Avenue, Glasgow, G12 8LT, U.K.
[b] L-NESS, Politecnico di Milano, Via Anzani 42, 22100, Como, Italy
[c] Johannes Kepler Universität, Institute of Semiconductor and Solid State Physics, Linz, Austria
[d] Paul Scherrer Institute, CH-5232 Villigen PSI, Switzerland

Low dimensional structures such as superlattices have the potential to improve the thermoelectric properties of materials by engineering the scattering of phonons to reduce the thermal conductivity and therefore improve the thermeoelectric performance. Here we demonstrate the reduction in thermal conductivity in Ge/SiGe superlattices using multiple barrier engineering to scatter acoustic phonons at the key wavelengths for thermal transport. The approach allows ZT to be increased in wide quantum well superlattices through the reduction of heterointerfaces which scatter both electrons and phonons.

Introduction

There is significant interest in improving the efficiency of thermoelectric generators to enable the harvesting of free thermal energy for powering a wide range of applications including autonomous sensors (1). Almost all commercially available thermoelectric generator or Peltier coolers are fabricated from BiTeSb alloys which have a figure of merit, ZT close to 1 at 100 ˚C (2). The key performance thermoelectric materials is characterized by the figures of merit $ZT = \alpha^2\sigma T/\kappa$ where α is the Seebeck coefficient, σ is the electrical conductivity, T is the temperature and κ is the thermal conductivity and the power factor defined as $\alpha^2\sigma$. Higher ZT results in higher thermodynamic conversion efficiencies but the power factor is also important for maximum power generation for a given load (1). For bulk materials, the Wiedemann-Franz rule links the thermal and electrical conductivities making improvements beyond the values achieved at the optimum doping level difficult (2).

If low dimensional structures or nanostructures are used, however, a number of new mechanisms can be used to potentially improve the ZT value and efficiency (3). Two standard approaches are typically used. The first uses nanowires (4), quantum dots (5) or superlattices (6) to add nanoscale scattering centers to reduce κ faster than σ. The second approach aims to enhance the asymmetry of the density of states across the chemical potential to enhance the Seebeck coefficient (7) again in superlattices, nanowires or

quantum dots. We have previously investigated ZT improvement over $Si_{1-x}Ge_x$ alloys (8) using $Ge/Si_{1-x}Ge_x$ superlattices both for lateral transport along p-type modulation doped Ge QWs (9) and vertical transport p-type $Ge/Si_{1-x}Ge_x$ superlattices (10).

In this work we investigate the impact of engineering phonon scattering on ZT and power factor. We deliberately pick a range of barriers in Ge/SiGe superlattices between 1.5 and 5 nm which is where most of the phonon wavelengths key to the transport of thermal energy in the material are located and in doing so attempt to reduce κ as calculated using a Callaway model for Si or Ge with all phonons (11) or only with acoustic phonons (12). This is demonstrated through selecting superlattice designs with 1 to 3 barriers which span the acoustic phonon wavelengths key for increasing the thermal transport of energy. The work also demonstrates how to reduce the number of heterointerfaces and in doing so how to increase ZT. This approach allows wider quantum well (QW) designs provide superior σ and power factors compared to narrow QW designs.

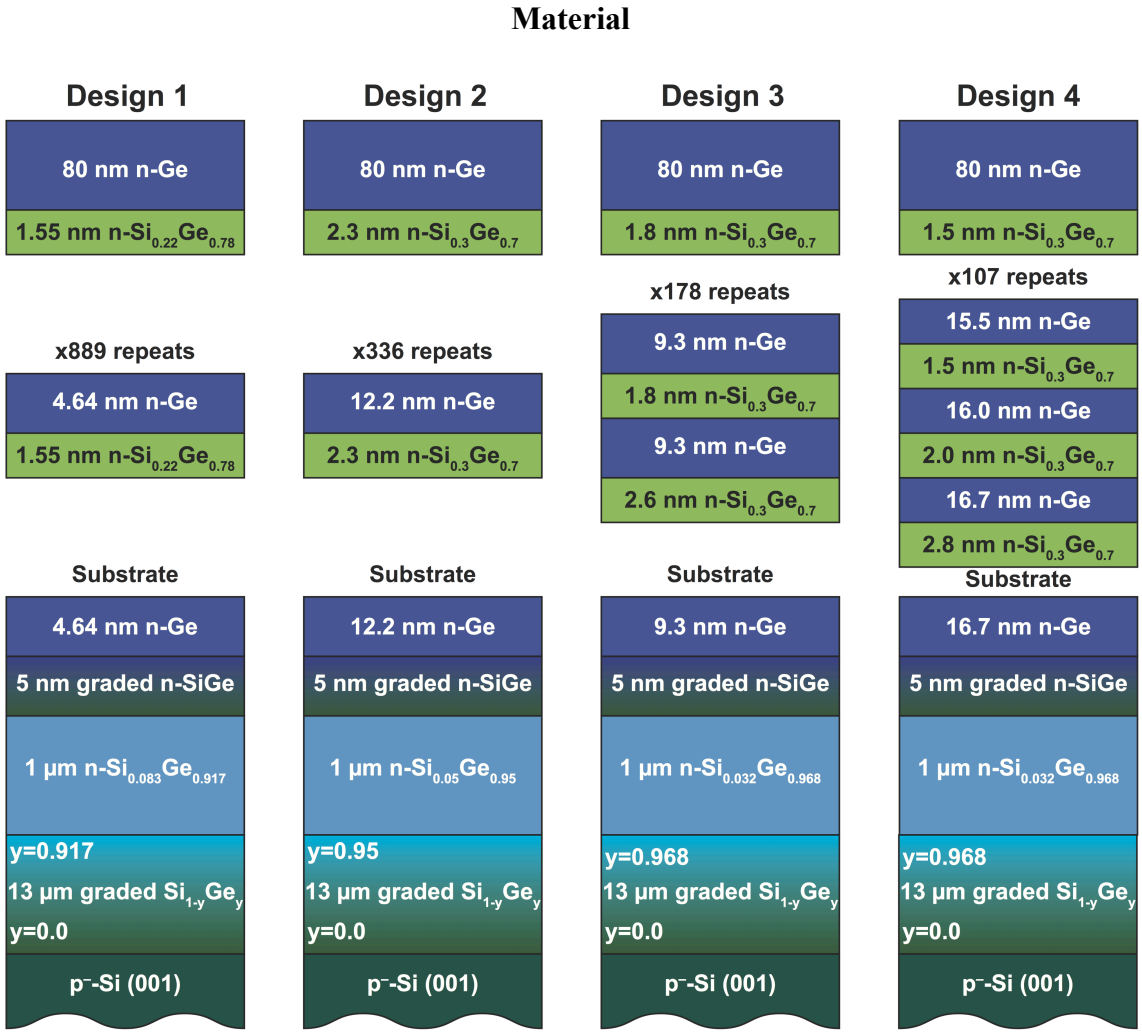

Figure 1. The heterolayer thicknesses and Ge compositions for the 4 wafer designs being investigated in this paper.

The designs use Ge and $Si_{1-x}Ge_x$ as QW and barriers to form superlattices. Ge has been used as the QW as it has a far higher ZT than Si (9)(10). Figure 1 present the 4 designs

used in this work. Designs 1 and 2 grow approximately similar thicknesses of superlattice material but Design 1 has narrower QWs and therefore Design 2 has 2.5 times fewer heterointerfaces. Designs 2, 3 and 4 have 1, 2 and 3 barriers with different thicknesses respectively.

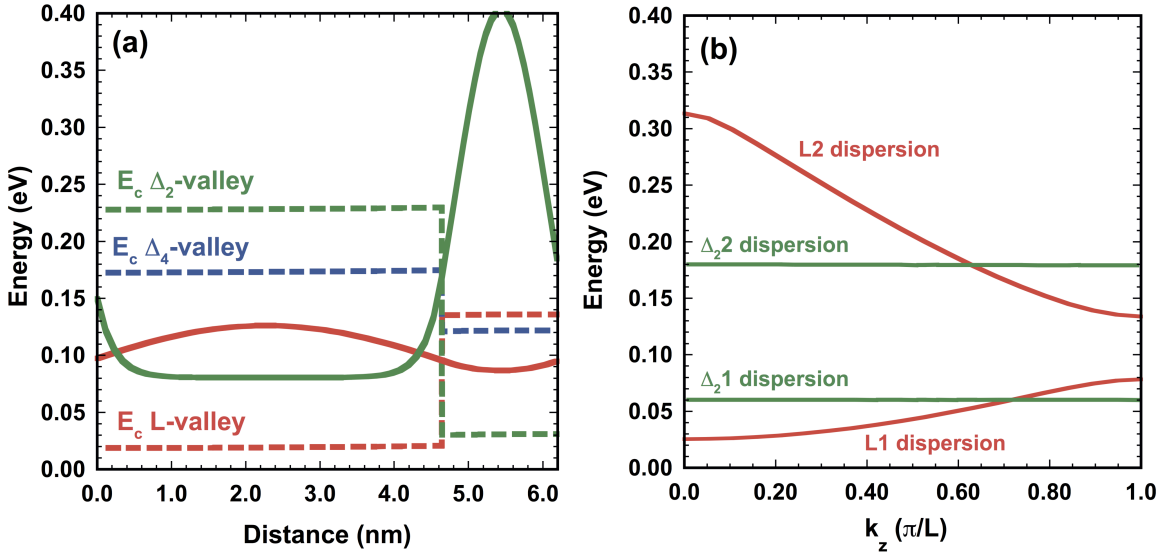

Figure 2. (a) The strain-split conduction band edges for a single period of the Design 1 sample with 4.64 nm Ge QW and 1.55 nm $Si_{0.22}Ge_{0.78}$ barrier superlattice grown on relaxed $Si_{0.083}Ge_{0.917}$. (b) The calculated superlattice dispersion for the L-valley and Δ_2-valley electron state where the Δ_2 mini band widths are both zero and the L1 mini band width is 54.3 meV.

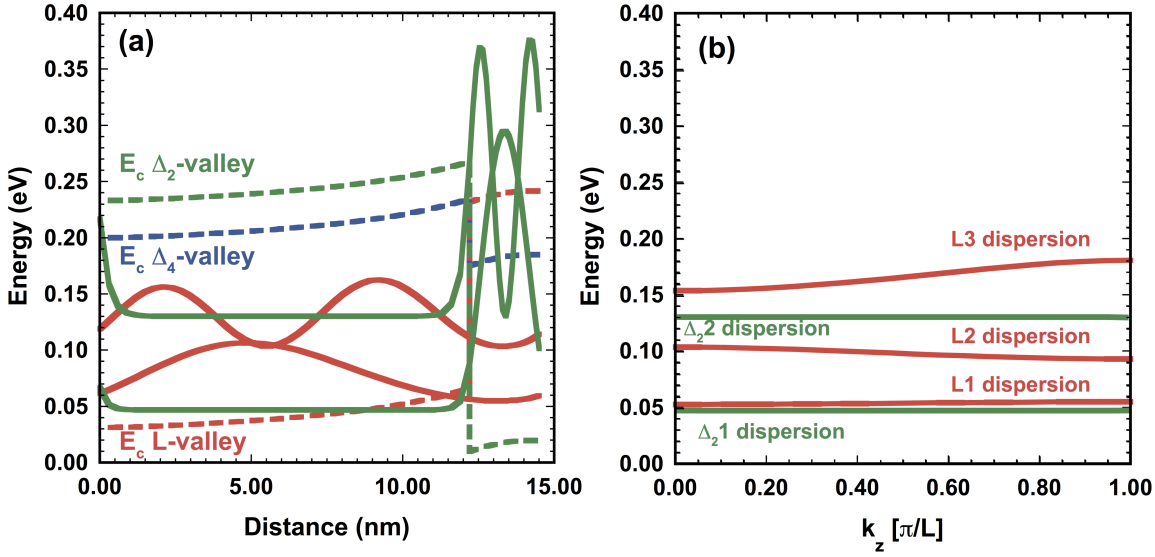

Figure 3. (a) The strain-split conduction band edges for a single period of the Design 2 sample with 12.2 nm Ge QW and 2.3 nm $Si_{0.30}Ge_{0.70}$ barrier superlattice grown on relaxed $Si_{0.05}Ge_{0.95}$. b) The calculated superlattice dispersion for the L- and Δ_2-valley electron miniband states where the Δ_2 miniband widths are both zero and the L1 miniband width is 2.5 meV.

All the material was grown on 100 mm diameter p-Si (001) substrates of 5-10 Ω-cm using low-energy plasma enhanced chemical vapour deposition (LE-PECVD) (13)(14). For all wafers, a strain relaxed graded buffer of ~13 µm thickness was grown at a rate of

between 5 and 10 nm/s. Once a bottom contact layer was grown the superlattices were grown at between 1.0 to 1.5 nm/s. The full heterolayer stacks are presented in Figure 1.

Figures 2 and 3 present the bandstructure and superlattice dispersions for Designs 1 and 2 respectively as calculated by an 8-band **k.p** Poisson-Schrödinger tool (15). For the narrower 4.64 nm QW of Design 1, the L-valley is the ground state in the QW with an effective mass, $m^* = 0.118\ m_0$ (where m_0 is the free electron mass) whilst in the barrier it is $0.139m_0$. The Δ_2-valley is the ground state forming a QW in the barrier to the Ge L-valley QWs but since $m^* > 1.2m_0$ in the barriers and QWs in the transport direction, the subband states are localized and there is no extended electron transport through these states, only scattering. This is clearly shown in the superlattice miniband dispersion where the Δ_2 miniband widths are both zero. The L-valley dispersion for the ground state miniband is 54.3 meV for the 4.64 nm QW in Figure 2(b) and this reduces to 2.5 meV for the 12.2 nm Ge QW in Figure 3(b).

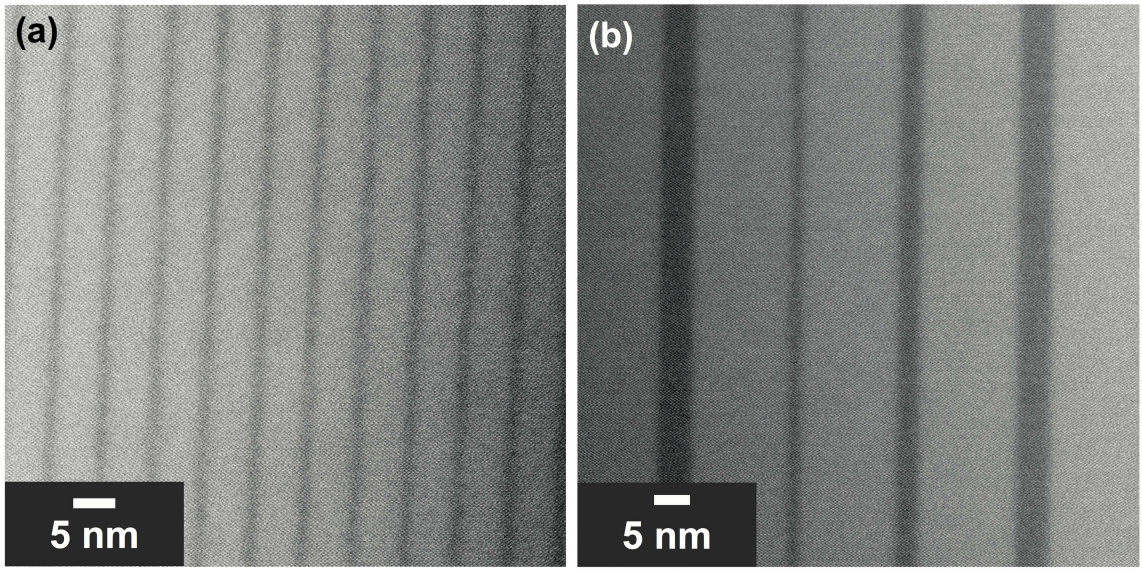

Figure 4. (a) A TEM image of Design 1 with a single barrier and QW. (b) A TEM image of Design 4 with 3 different barrier and QW thicknesses.

The superlattice designs were investigated in a Tecnai F30ST TEM operated at 300 kV (FEI, 0.19 nm point-to-point resolution), and a HD-2700Cs dedicated, Cs-corrected scanning TEM operated at 200 kV (Hitachi, 0.078 nm resolution). The samples were prepared by conventional cross-section preparation (mechanical pre-preparation and Ar-ion etching). Figure 4 demonstrates TEM images from (a) Design 1 and (b) Design 4. The Design 4 TEM images clearly shows the 3 different $Si_{0.3}Ge_{0.7}$ barrier thicknesses of 1.5, 2.0 and 2.8 nm with Ge QW widths of 15.5, 16.0 and 16.7 nm. In all cases the TEM indicates an interface roughness of about 4 monolayer which corresponds to a height roughness, Δ of 0.56 nm. This should be compared to previously reported interface roughness in quantum cascade superlattice material of $Si/Si_{0.2}Ge_{0.8}$ with $\Delta = 0.4$ nm and a lateral correlation length, Λ of 2.3 nm (16).

High resolution x-ray diffraction (HRXRD) measurements were used to characterize the heterolayer composition, strain, thickness and quality using analysis of line scans along Q_z and reciprocal space maps (RSMs) obtained around the (004) and (224) Bragg reflections. The measurements were performed using a PANalytical X'Pert PRO MRD

high-resolution X-ray diffractometer: the system is equipped with a hybrid mirror and 2-bounce asymmetric Ge monochromator for a high-intensity Cu Kα 1 beam (λ = 0.1540562 nm). For device processing and thermoelectrical characterization it is particularly important to know the thickness of the multi-QW samples at every point across the 100 mm wafer, which is mapped by taking (004) ω − 2θ scans on a 1 × 1 cm grid. The bending of the substrate, associated with the tensile strain developed during cool down from the deposition temperature is measured from the shift in the ω position of the substrate (004) Bragg peak across the wafer (17).

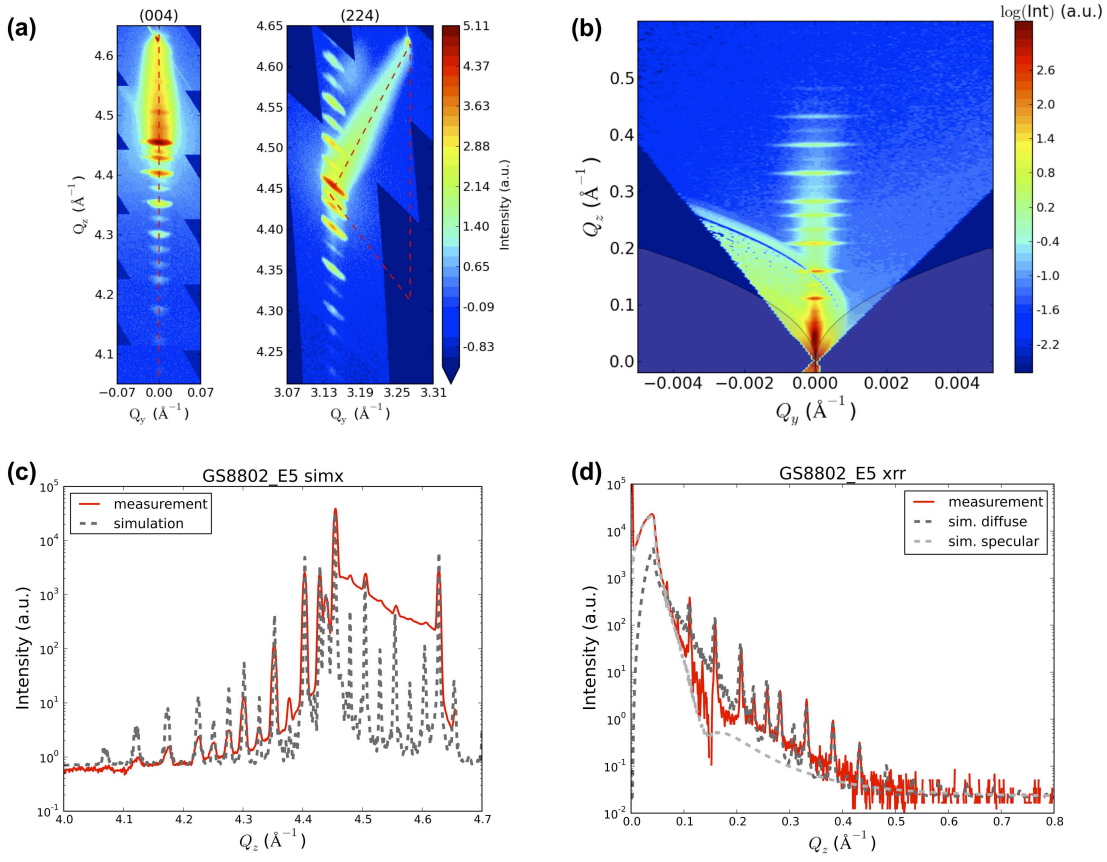

Figure 5. (a) XRD scans along (004) and (224) and (b) XRR reciprocal map for the Design 3. (c) and (d) show the simulation results compared to the data measured for XRD and XRR scans.

Figure 5(a) presents the (004) and (224) HRXRD scans for Design 3 which has 2 barriers whilst Figure 5(c) presents the results of the simulations to extra the key heterolayer parameter thicknesses and Ge compositions. Figure 5(b) presents the x-ray reflectivity (XRR) experimental measurements which are compared to the simulatations in Figure 5(d). In all cases the heterolayer thicknesses extracted from the HRXRD simulations agreed within experimental error (i.e. to with about 0.3 nm) to the TEM results in Figure 4. Again the HRXRD suggested an interface height roughness, Δ of about 4 monolayers.

Microfabricated Devices for Thermoelectric Performance Measurements

Figure 6 presents cartoons of the two devices microfabricated to allow the extraction of the α and κ values. Photolithography was used before a mesa pattern was etched using

SF_6 and C_4F_8 mixed etch process (18) which has demonstrated very low levels of damage (19). Metal contacts were patterned using Ag (1% Sb) annealed at 400 ˚C at the top and bottom of the mesa to provide electrical Ohmic contacts (20). On top of the mesa a thin 50 nm Si_3N_4 layer is deposited by PECVD before a four terminal thermometer was deposited using Ti/Pt metals. 30 nm of further Si_3N_4 was deposited before a top heater of NiCr. A bottom Ti/Pt four terminal thermometer and bottom Ohmic was also patterned.

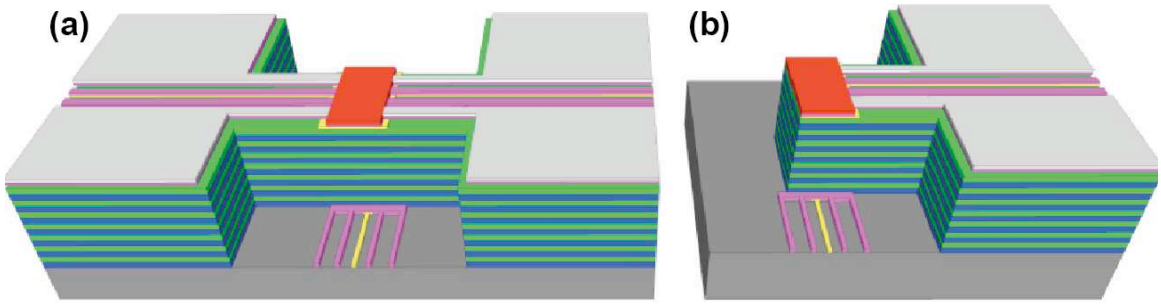

Figure 6. (a) A full microfabricated device for the extraction of α and κ with a top heater (red), thermometer (pink) and electrical contacts (yellow). At the bottom of the device is a second thermometer (pink) to extract ΔT across the device and a second electrical contact (yellow). (b) A half device with only half the electrical connections and superlattice material that conducts heat away from the material test area. This is designed to allow the parasitic thermal contribution through the electrical connections and side material to be estimated from measurements (10).

The full device is fabricated which has a heater at the top and electrical connections top and bottom allow the Seebeck voltage, ΔV between the contacts to be measured (Figure 6(a)). To get an absolute Seebeck voltage the metal Seebeck coefficients of 1.51 $\mu V/K$ must be subtracted (21). A set of calibrated Ti/Pt four-terminal thermometers top and bottom allows the ΔT to be measured. This device will allow measurements but they are perturbed by the thermal transport of heat through the electrical connections and all material at the side of the mesa that is required to make electrical contacts to the top heater, top electrical contact and the top thermometer contacts. To remove this inaccuracy, a second half structure is also fabricated (Figure 6 (b)) where only half the parasitic thermal load is present. By measuring both and undertaking simulations to remove all the parasitic thermal loads, significantly more accurate values for α and κ can be obtained.

Figure 7 (a) presents a comparison between the experimentally measured Seebeck coefficient and simulations using Comsol (21). The simulation accounts for the parasitic channels as indicated in Figures 7(b) and (c) where the simulation allows an estimate of the amount of heat lost to the parasitic thermal conduction paths at the side of the mesa and through the electrical interconnects for a given 100 mW of power to the top heater. Figure 7(d) presents the Seebeck voltage through the device achieved with the same 100 mW of heater power being applied as (b) and (c). The experiments and simulations agree to within 10% indicating that the simulations do help to reduce the uncertainty from parasitic channels. For κ, the simulations validated using the full and half microfabricated devices indicate that only 67% of the heat goes through the section of material under test (the cuboid directly under the heater) and 33% is conducted away through the parasitic channels. From a measurement of a reference samples of SiO_2 a κ of 1.7 ± 0.6 $Wm^{-1}K^{-1}$ was deduced, which compares well with literature values of 1.6 $Wm^{-1}K^{-1}$ (22) providing confidence in the accuracy of the technique.

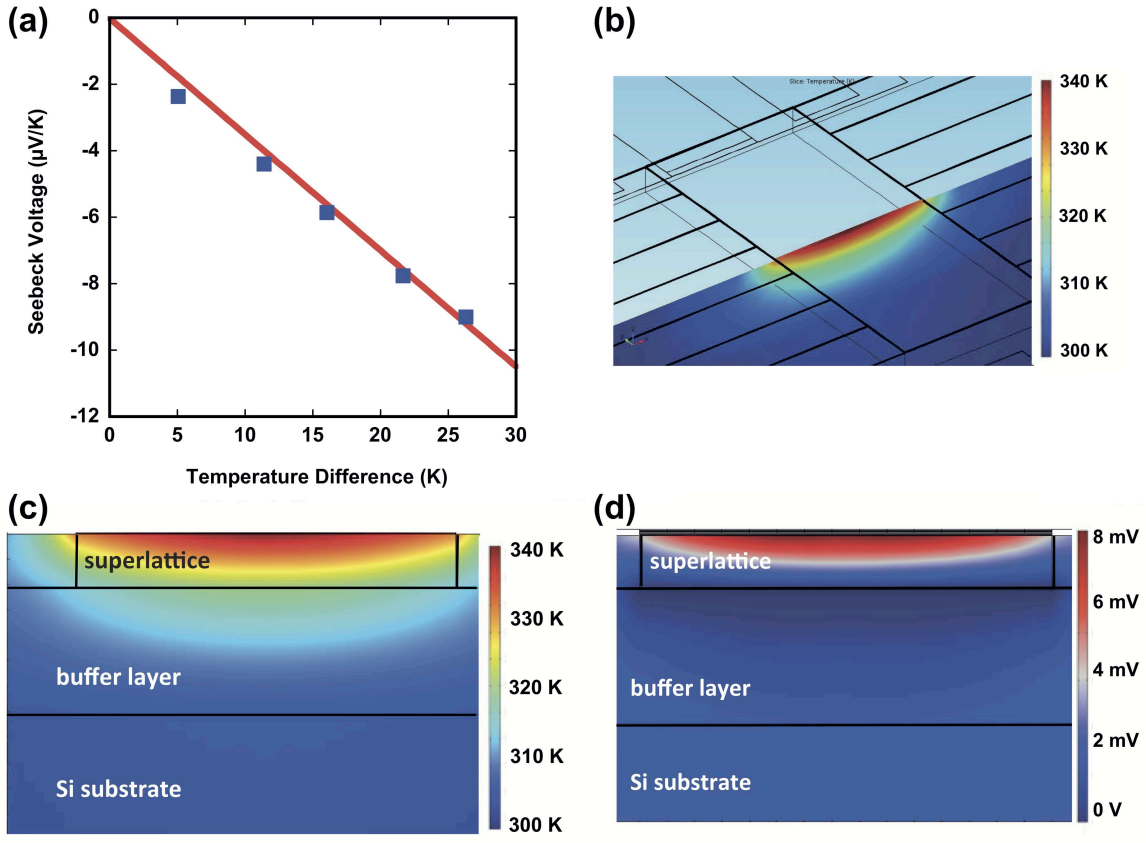

Figure 7. (a) A comparison between the Seebeck voltage both measured and simulated. The simulation and measurements agree to within 10%. (b) A plot demonstrating the simulated temperature profile of the plane chosen in the middle of the device, while (c) shows a cross section of the same plane. (d) A plot of the simulated Seebeck voltage across the same plane as the temperature in plot (c).

The cross plane (vertical) σ was extracted using a range of circular transfer line measurement structures (23) etched to a range of depths from 0 to 5 μm as described in refs. (10)(24). The devices were measured as function of the gap spacing for 8 different heights up to the superlattice thickness of 5 μm. For each of these 8 intercept resistances, (when the gap spacing was 0 μm) was extracted and plotted as a function of the etch depth. The gradient of these data points allows σ to be extracted. The results are presented in Figure 8 and Table 1.

Thermoelectric Performance

Figure 8(a) presents σ and κ as the number of barriers increases from 1 to 3. A clear decrease in κ is observed. As the number of heterostructures reduces from Design 2 to Design 4 this is clearly not related to just heterointerface scattering. σ also reduces and so the ZT values remain approximately constant over all three Designs. Of more concern for applications is that the power factor also reduces as the number of barrier widths increase. Table 1 also indicates that the lowest κ comes from Design 1 with the largest number of heterointerfaces but the value is close to Design 4 with under half the number. Finally Design 1 had a small σ compared to Design 2 so wider QWs are certainly better for higher electrical conductivity.

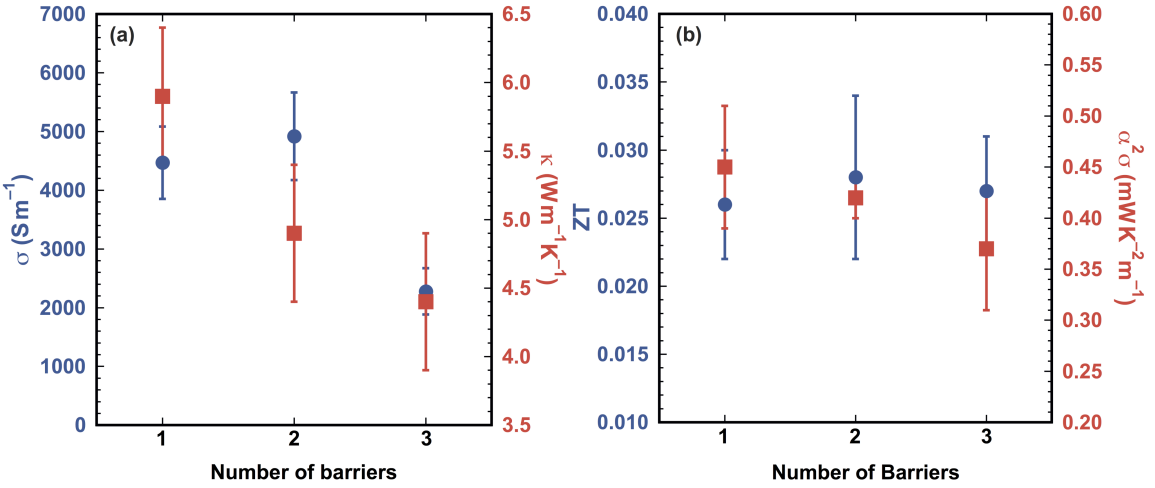

Figure 8. (a) The electrical conductivity (circles) and thermal conductivity (squares) at 300 K for the Designs 2,3 and 4 with 1, 2 and 3 barriers respectively. (b) The ZT (circles) and power factor (squares) at 300 K for the Designs 2,3 and 4 with 1, 2 and 3 barriers respectively.

TABLE I. The key thermoelectric parameters for Designs 1 to 4 compared to other materials in the literature.

Material	S (Sm^{-1})	α (μVK^{-1})	κ ($Wm^{-1}K^{-1}$)	ZT
Design 1	1,834 ± 287	–455 ± 23	4.3 ± 0.7	0.028 ± 0.003
Design 2	4,471 ± 616	–320 ± 4	5.9 ± 0.5	0.026 ± 0.004
Design 3	4,918 ± 745	–295 ± 33	4.9 ± 0.5	0.028 ± 0.006
Design 4	2,277 ± 394	–403 ± 3	4.4 ± 0.5	0.027± 0.004
n-Ge (8)	66,700	–155	59.9	0.008
n-$Si_{0.7}Ge_{0.3}$ (8)	31,300	–258	5.6	0.112
n-$Si_{0.2}Ge_{0.8}$ (8)	38,400	–240	8.9	0.075
n-Si/Ge (25)	400	–620	12.5	0.004
n-Si/$Si_{0.7}Ge_{0.3}$ (26)	9,800	–297.5	–	–

With further analysis for all the designs, it would appear that while both σ and κ are significantly below the alloy value for comparable Ge content bulk $Si_{0.2}Ge_{0.8}$ material (8), σ has reduced to a much greater extent that κ. Therefore whilst the ZT values produced are greater than bulk Ge, the ZT values are all below the equivalent bulk alloy value of n-$Si_{0.2}Ge_{0.8}$ (8). Analysis suggests that the 0.56 nm of interface roughness may be the reason. For vertical transport, interface roughness scattering decreases the electrical conductivity as the square of the interface roughness height, Δ (27). Typical roughness for GaAs/AlGaAs superlattices is around 1 monolayer which is significantly lower than the 4 monolayers in the present material. Interface roughness clearly reduces σ but it also reduces κ as demonstrated with Ge quantum dots with a wetting layer in a Si matrix (5).

Conclusions

An approach to reduce κ using multiple SiGe barriers in a Ge matrix to scatter a range of acoustic phonons at different wavelengths has been successfully demonstrated. A high level of interface roughness of 4 monolayers in the Ge/SiGe superlattice results in σ being reduced at a faster level than κ. This results in ZT values for the superlattices which are higher than bulk Ge but lower than the equivalent bulk alloy n-$Si_{0.2}Ge_{0.8}$.

Clearly optimized heterolayers with smoother heterointerfaces will be required if higher electrical conductivity and higher ZTs are to be achieved with this approach. This work demonstrates the importance of measuring all the α, σ and κ thermoelectric parameters when assessing the potential improvements in ZT from a particular approach. The approach, however, also allows ZT to be increased in wide quantum well superlattices through the reduction of heterointerfaces which scatter both electrons and phonons. This suggests ways forward for better designs with higher thermoelectric performance where only a few barriers in very wide QWs are used to increase σ in the material whilst maintaining a low κ.

Acknowledgments

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